I. AMENDMENT

In the Claims:

Please amend claims 1, 7-8, 13, 17, and 20-21 as follows:

1. (currently amended) An integrated circuit, comprising:

functional-circuit blocks that are spaced apart from one another, each block
having a respective boundary that surrounds the block;

a region disposed outside of the boundaries of the functional-circuit blocks
and devoid of functional-circuit blocks; and

a transistor disposed in the region and having been placed in the region
during the design of the integrated circuit after the functional-circuit
blocks were placed.

2. (previously presented) The integrated circuit of claim 1 wherein one of the
functional-circuit blocks is configured to perform a predetermined function.

3. (allowed) An integrated circuit, comprising:

functional-circuit blocks that are spaced apart from one another;

a region disposed between the functional-circuit blocks and devoid of
functional-circuit blocks;

a transistor disposed in the region; and

wherein one of the functional-circuit blocks is unconfigured.

4. (original) The integrated circuit of claim 1 wherein the transistor comprises
an FET transistor.

5. (allowed) An integrated circuit, comprising:

functional-circuit blocks that are spaced apart from one another;

a region disposed between the functional-circuit blocks and devoid of
functional-circuit blocks;

a transistor disposed in the region; and

wherein the transistor is automatically placed in the devoid region after the
functional-circuit blocks are placed.

2

6. (allowed) An integrated circuit, comprising:

functional-circuit blocks that are spaced apart from one another;

a region disposed between the functional-circuit blocks and devoid of

functional-circuit blocks;

a transistor disposed in the region; and

wherein the transistor is manually placed in the devoid region after the

functional-circuit blocks are placed.

7. (currently amended) An integrated circuit, comprising:

functional-circuit blocks that are spaced apart from one another, each block

having a respective boundary that surrounds the block;

a region located between and outside the boundaries of the functional-circuit

blocks, and devoid of functional-circuit blocks, and defined during the

design of the integrated circuit after the locations of the

functional-circuit blocks were defined; and

a buffer disposed in the region and coupled to one of the functional-circuit

blocks.

8. (currently amended) An integrated circuit, comprising:

functional-circuit blocks that are spaced apart from one another, each block

having a respective boundary that surrounds the block;

a region located between and outside the boundaries of the functional-circuit

blocks, and devoid of functional-circuit blocks, and defined during the

design of the integrated circuit after the locations of the

functional-circuit blocks were defined; and

a logic circuit disposed in the region and coupled to one of the

functional-circuit blocks.

9. (original) The integrated circuit of claim 8 wherein the logic circuit

comprises a logic gate.

10. (original) The integrated circuit of claim 8 wherein the logic circuit

comprises an inverter.

3

11. (allowed) An integrated circuit, comprising:

first and second supply nodes;

functional-circuit blocks that are spaced apart from one another, one of the
   functional-circuit blocks coupled to the first and second supply nodes;

a region located between the functional-circuit blocks and devoid of
   functional-circuit blocks; and

a transistor disposed in the region and having a pair of input-output terminals
   coupled to the first supply node and having a control terminal coupled
   to the second supply node.

12. (allowed) The integrated circuit of claim 11 wherein:

the transistor comprises an FET transistor;

the pair of input-output terminals comprises a pair of source-drain terminals;
   and

the control terminal comprises a gate terminal.

13. (currently amended) An integrated circuit, comprising:

a conductive path;

functional-circuit blocks that are spaced apart from one another, each of the
   blocks having a respective boundary that surrounds the block, one of
   the functional-circuit blocks coupled to the conductive path;

a region located between and outside the boundaries of the functional-circuit
   blocks and devoid of functional-circuit blocks; and

a transistor disposed in the region and having a pair of input-output terminals
   coupled to the conductive path and having a control terminal, the
   transistor having been designated for disposition in the region during
   the design of the integrated circuit after the functional-circuit blocks
   were designated for disposition in respective locations of the integrated
   circuit.

14. (original) The integrated circuit of claim 13, further comprising:

a supply node; and

wherein the control terminal is coupled to the supply node.

4

15. (original) The integrated circuit of claim 13 wherein the control terminal is coupled to one of the input-output terminals.

16. (original) The integrated circuit of claim 13 wherein the control terminal is short-circuited to one of the input-output terminals.

17. (currently amended) An integrated circuit, comprising:

first and second regions that are spaced apart from one another and that
      have first and second boundaries that respectively surround the first
      and second and second regions;

first and second functional-circuit blocks respectively disposed in the first and
      second regions and entirely within the first and second boundaries;

a third region located between the first and second functional-circuit blocks
      and outside of the first and second boundaries and devoid of
      functional-circuit blocks, the third region having been defined during
      the design of the integrated circuit after the first and second
      functional-circuit blocks had been designated for disposition in the first
      and second regions;

a buffer disposed in the third region and having an input terminal and an
      output terminal;

a first conductive path having a first terminal coupled to the first
      functional-circuit block and having a second terminal coupled to the
      input terminal of the buffer; and

a second conductive path having a first terminal coupled to the output
      terminal of the buffer and having a second terminal coupled to the
      second functional-circuit block.

18. (previously presented) The integrated circuit of claim 17 wherein the first
      and second functional-circuit blocks are operable to perform first and
      second predetermined functions, respectively.

19. (previously presented) The integrated circuit of claim 17, further
      comprising:

a supply node; and

5

wherein the buffer comprises a transistor disposed in the third region and having a control terminal coupled to the input terminal of the buffer, a first terminal coupled to the output terminal of the buffer, and a second terminal coupled to the supply node.

20. (currently amended) An integrated circuit, comprising:

first and second regions that are spaced apart from one another and that have first and second boundaries that respectively surround the first and second and second regions;

first and second functional-circuit blocks that are respectively disposed in the first and second regions and entirely within the first and second boundaries;

a third region located between the functional-circuit blocks and outside of the first and second boundaries, and devoid of functional-circuit blocks, the third region having been defined during the design of the integrated circuit after the first and second functional-circuit blocks had been designated for disposition in the first and second regions;

a logic circuit disposed in the third region and having an input terminal and an output terminal;

a first conductive path having a first terminal coupled to the first functional-circuit block and having a second terminal coupled to the input terminal of the logic circuit; and

a second conductive path having a first terminal coupled to the output terminal of the logic circuit and having a second terminal coupled to the second functional-circuit block.

21. (currently amended) An integrated circuit, comprising:

functional-circuit blocks spaced apart from one another and each having a respective boundary that surrounds the block;

a region located between and outside the boundaries of the functional-circuit blocks and devoid of functional-circuit blocks; and

a repair transistor disposed in the region and having a three terminals, one of the terminals coupled to one of the functional-circuit blocks, the repair transistor having been placed in the region during the design of the integrated circuit after the placement of the functional-circuit blocks.

6

22. (previously presented) The integrated circuit of claim 21 wherein two of
the transistor terminals are coupled to the one functional-circuit block.

23. (previously presented) The integrated circuit of claim 21 wherein the three
transistor terminals are coupled to the one functional-circuit block.

24. - 43. (cancelled)